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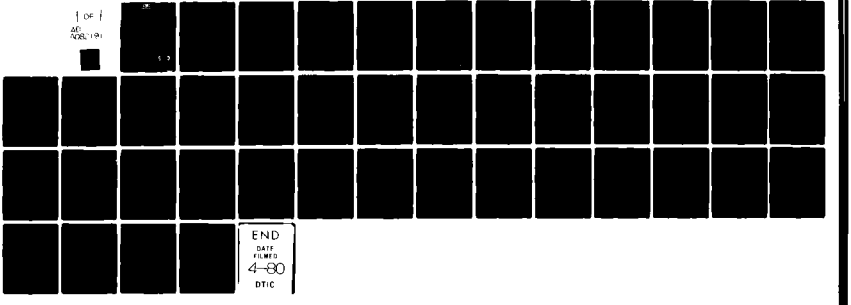

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MOS MEASUREMENT METHODS

Design Principles for a Radiation-Hardened CMOS/SOS Memory

Rockwell International Corporation
P.O. Box 3105
Anaheim, California 92803

1 February 1979

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The survival of data in a memory through very high levels of transient ionizing radiation (>10^{11} rads(Si)/sec) has been a very difficult problem. This report describes the principles used in the design of a hardened memory, using CMOS/SOS technology. The design also provides high packing density (1024 bits in less than 16000 $mils^2$), high speed (cycle time <350 nsec), low power (<50 mW) and ease of use (16 pin packaging with a single-chip enable clock).

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ILLUSTRATIONS

I. INTRODUCTION

This report describes the key considerations that were involved in the conceptual design of a 1024-bit silicon gate CMOS/SOS state retention random access memory. Three appendices are attached to the report. Appendix I describes the design rules used to define the topological layout of key memory areas. In Appendix II, a radiation-hardened CMOS/SOS process is outlined. Appendix III contains data describing the total-dose radiation response of CMOS/SOS devices fabricated with the process outlined in Appendix II.

II. RADIATION CONSIDERATIONS

Semiconductor memories which combine nuclear radiation hardness with the high density, speed and low power-dissipation of state-of-the-art large-scale-integrated (LSI) circuits are not presently available for many systems which now have such requirements. Radiation-induced changes in device parameters limit the operational range of "state-of-the-art" LSI random access memories (RAMs) to about 5×10^3 rads(Si) total dose and 3×10^9 rads(Si)/sec transient dose rate.[1] Over the past several years, there have been a number of publications on the subject of integrated-circuit radiation hardening. Most of these publications address process approaches. Process modifications, with minimum design and layout changes, have allowed some increases in the hardness of available LSI designs. Also, some small capacity RAMs have been specifically designed and fabricated to withstand higher radiation levels. In the first case, the increase in radiation hardness is generally not satisfactory for most applications. In the second case, the small storage capacity (e.g., 64 bits) per chip limits applicability.

To achieve the radiation hardness goals shown in Table 1 along with an access time below 300 nsec, both hardened processes and hardened circuit-design methods are necessary.

The main objective of this program was to identify methods for achieving a high degree of radiation hardness with minimum sacrifice of the density and performance of LSI random access memories (RAMs).

Radiation-hardened designs must consider three different types of effects--(1) permanent ionizing-radiation degradation of MOS device parameters, (2) transient upset of operation and (3) damage due to neutron fluence.

The permanent degradation[2-7] in MOS device characteristics is caused by accumulated ionizing radiation dose effects--resulting in shifts of threshold voltages, increases in leakage currents, decreases in gain, and changes in various other parameters. The degradation of these device parameters varies with the individual MOS device and depends upon the voltage bias existing during the time of the radiation exposure. Some annealing of the degradation may occur with time and temperature.

The transient upset of operation is induced by short-pulse high-dose-rate radiation events, which result in radiation-generated photocurrents and temporary shifts of MOS device parameters. After a recovery time, the currents and parameters return approximately to their original values; however, the disturbances can cause a loss of information or "scrambling" of a memory.

The effects of neutron fluence on MOS devices (up to at least 10^{15} neutron/cm^2) are generally not significant.

The use of radiation hardened, silicon gate CMOS/SOS processes has greatly reduced the problems associated with threshold voltage variations and device leakages.[3-7] Nevertheless, circuit designs for 10^6 rads(Si) ionizing radiation dose must consider up to 4 V bias-dependent, nonuniform changes in threshold voltages (Figure 1).

Since, on a given chip, the threshold voltage of the individual MOS devices can be significantly different, the technique of threshold voltage control by substrate biasing circuits[8,9] is not adequate. Some designs must also allow up to 200 nA/μ drain-source leakage current (Figure 2), which also depends on device type and voltage bias. Degradations in carrier mobility and other parameters must also be tolerated in circuit operation.

Operation during high-level transient radiation is often not necessary, because an external radiation detector may switch off the logic circuits and "disconnect" the memory for the time of the exposure and recovery.

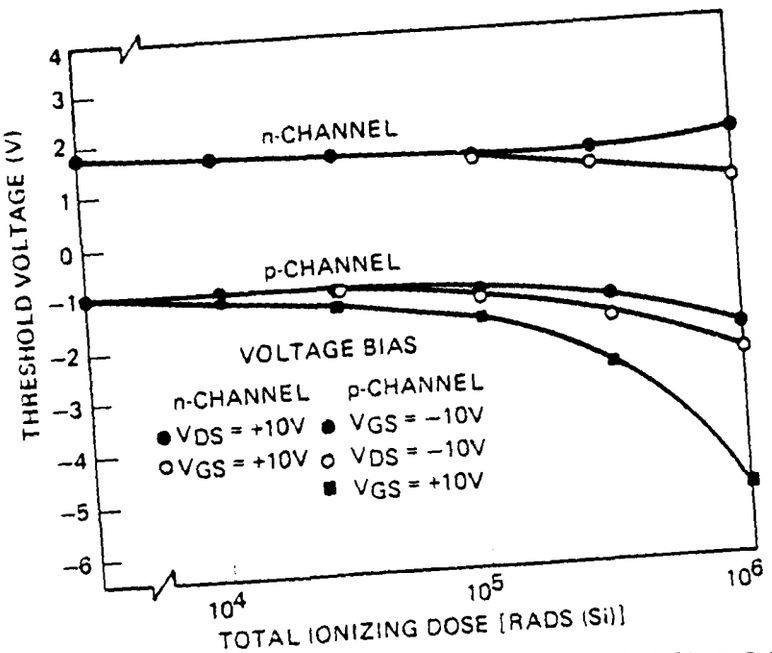

Figure 1. Effect of Radiation on Threshold Voltages for Different Bias Conditions

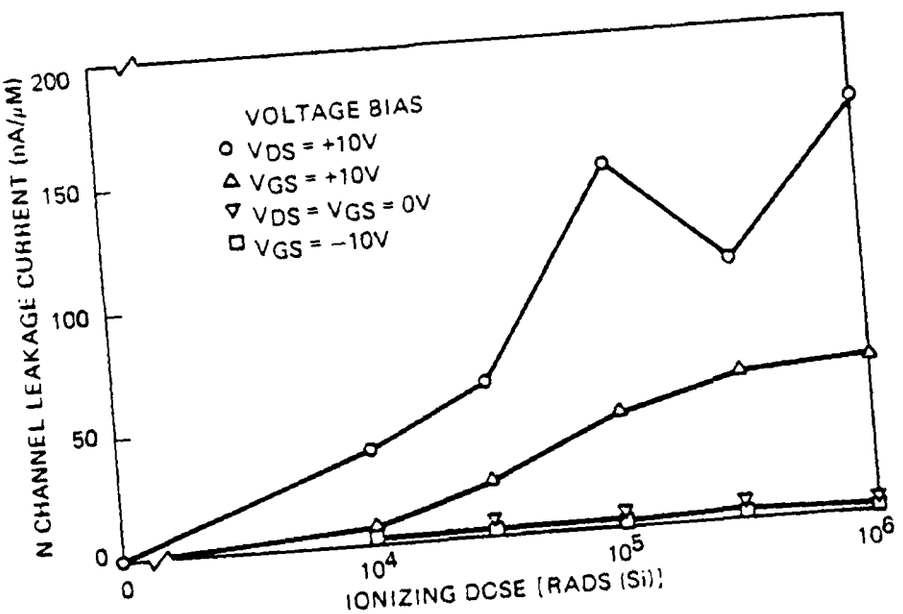

Figure 2. N-Channel Drain Leakage as a Function of Radiation Dose and Voltage Bias

However, beyond some specific dose rate (e.g., 10^9 - 10^{10} rads(Si)/sec), the memory cells can lose stored information due to high photocurrents (as much as 10 mA/mil) and transient threshold-voltage shifts beyond the value of supply voltages.[10-11]

III. GENERAL DESIGN CONSIDERATIONS

In addition to the radiation effects, the design must accommodate worst-case process tolerances, power supply and temperature variations. Thus, circuits designed for radiation hardness, as well as for normal variations, must tolerate a considerably larger range of parameter spreads and nonuniformities than those designed for commericial or military specifications only. E.g., Figure 3 shows a comparison of threshold

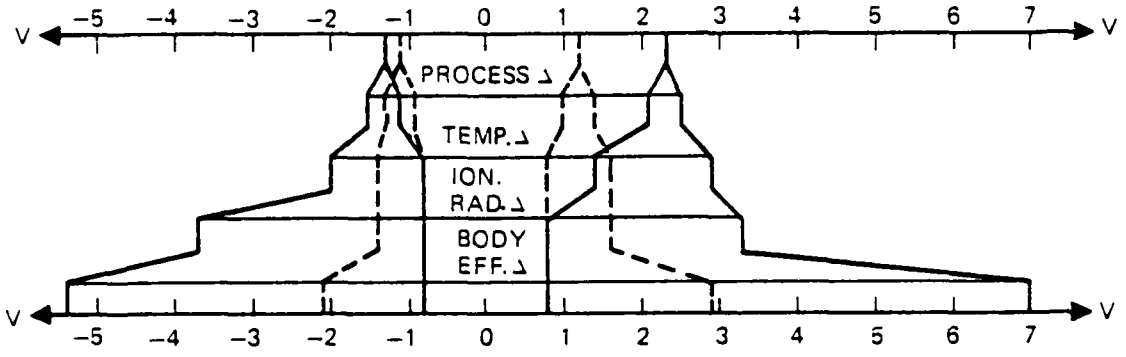

Figure 3. Threshold Voltage Ranges for Radiation Hardened Design (Solid Line) and Standard Design (Dotted Line)

voltage ranges for radiation-hardened and nonhardened designs. Consequently, the circuit design of a radiation-hardened CMOS/SOS RAM, which includes digital and analog stages on the same monolithic chip, should provide the following features:

- Compensation to decrease the effects of parameter degradation on the operation of the circuits.
- Balanced or differential circuitry in the highly sensitive analog functions which will provide a high degree of parameter tracking.

- Minimum sensitivity to timing of any floating nodes, to assure proper control of sensitive nodes during transient radiation pulses.
- Avoidance of circuitry configurations (e.g., NOR gates) which can become severely degraded after radiation exposure.

Inclusion of the above features in a radiation-hardened design will reduce the range of variations shown in Figure 3. Also, a parameter spread or range chart for each critical circuit area can be constructed. The following discussions highlight some of the important design considerations for each critical circuit area.

IV. MEMORY CELL DESIGN

The basic objective in the design of memory cells and a cell matrix is to achieve high density while tolerating a high ionizing radiation fluence [$\sim 10^6$ rads(Si)] and a high transient ionizing radiation pulse [$\sim 10^{12}$ rads(Si)/sec]. The high-density objective addresses not only small cell and matrix sizes, but also a minimum number of small-size peripheral circuits (e.g., sense amplifiers, drivers, etc.). A significant factor, then, is the ratio of the worst-case n-channel drive current to the post-radiation drain-source leakage. Practically, this ratio defines the maximum number of cells which can be tied to a given data bus line. (A small number of cells on a bus line implies more peripheral circuitry and lower density.) After irradiation, the drain-source leakage on an n-channel device may be an order of magnitude larger than that of a p-channel device;[3-7] therefore, p-channel devices normally would be selected as transfer elements for radiation hardened cells. Since the p-channel devices in this configuration can experience a worst-case bias condition, the threshold shifts may be large at the maximum radiation fluence. Excessively large threshold shifts will render the memory inoperatiave--especially if a 5-volt power supply is used. In addition, for operation at 10 volts, a special circuit configuration, with bias interruption on the selected column, would be required to overcome the write-in and speed difficulties created by the low drive current of the p-channel devices after irradiation.

To avoid these problems, n-channel devices with special design and process features can be used for transfer elements. These design and process features involve the special treatment of the edges of these n-channel devices, to minimize the radiation-induced leakage currents. The trade-off penalty is the inherent addition of some capacitances to the word lines. This capacitance causes the addressing to be slower.

Tolerance of the memory cells to high transient pulses of ionizing radiation can be realized by adding an RC stiffening network to a basic six-transistor complementary cell. Schematics of several different configurations of these types of memory cells are shown in Figure 4. These cells retain the information as a charge difference on the capacitor, C, during the generation and recovery of extremely high photocurrents.[11] After the disappearance of the radiation pulse and the resulting photocurrents, the storage flip-flop is forced back to its original state. The design shown in Figure 4(a) provides a balanced structure with a high degree of state retention. Particular attention must be given to the choice of physical structures for the resistors and capacitors in the cell. The capacitor structure must not suffer excessive discharge during the radiation pulse. An oxide-nitride sandwich structure can be used to minimize radiation-induced discharge and maximize capacitance per unit area. The doping levels of the resistors must be high enough ($\sim$2 kΩ/$\square$) so that the effects of ionizing radiation on the carrier concentration (conductivity modulation) is minimized. Finally, the RC time constant will determine the width of the radiation pulse that can be survived. Generally, the RC should be chosen to be about equal to the half-maximum width of the most intense radiation pulse. The values of resistance should be large enough to control the charging current to the capacitor when writing the cell.

A candidate layout for a state retention (RC) memory cell is shown in Figure 5. The area of this cell, using the design rules listed in Appendix I, is about 5 mils^2. The parameters of this cell (Table 2) can be used to calculate the various resistive and capacitive loads that must be considered in the design of the word drivers, the bit line and sense circuitry. Each cell contains an RC network like that shown in Figure 6.

Table 1. State Retention Memory Goals

Organization	1024 x 1
Total Dose	10^6 rads(Si)
Memory Retention	10^{12} rads(Si)/sec (30 nsec FWHM)
Neutron Fluence	10^{15} n/cm^2
Read Access - 100 nsec Cycle Time - 160 nsec	Post 3 x 10^5 rads(Si)

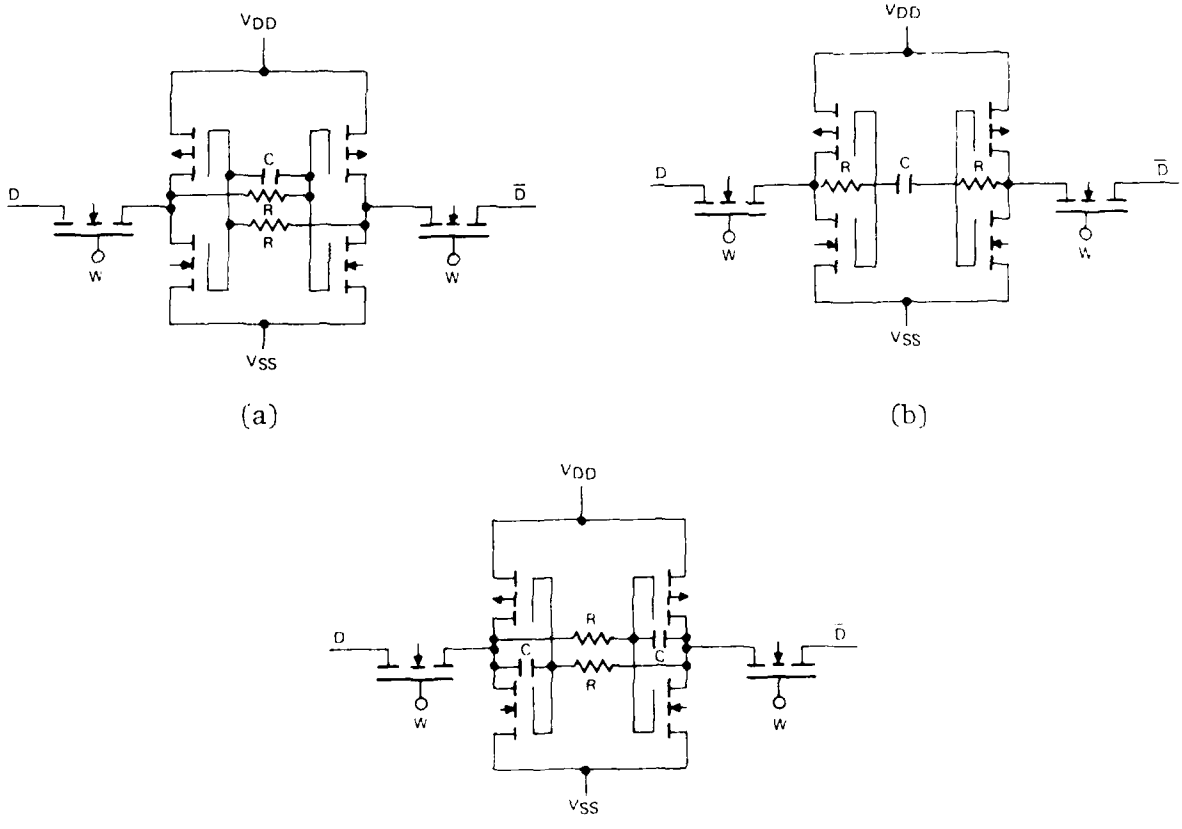

Figure 4. State Retention Type Memory Cells

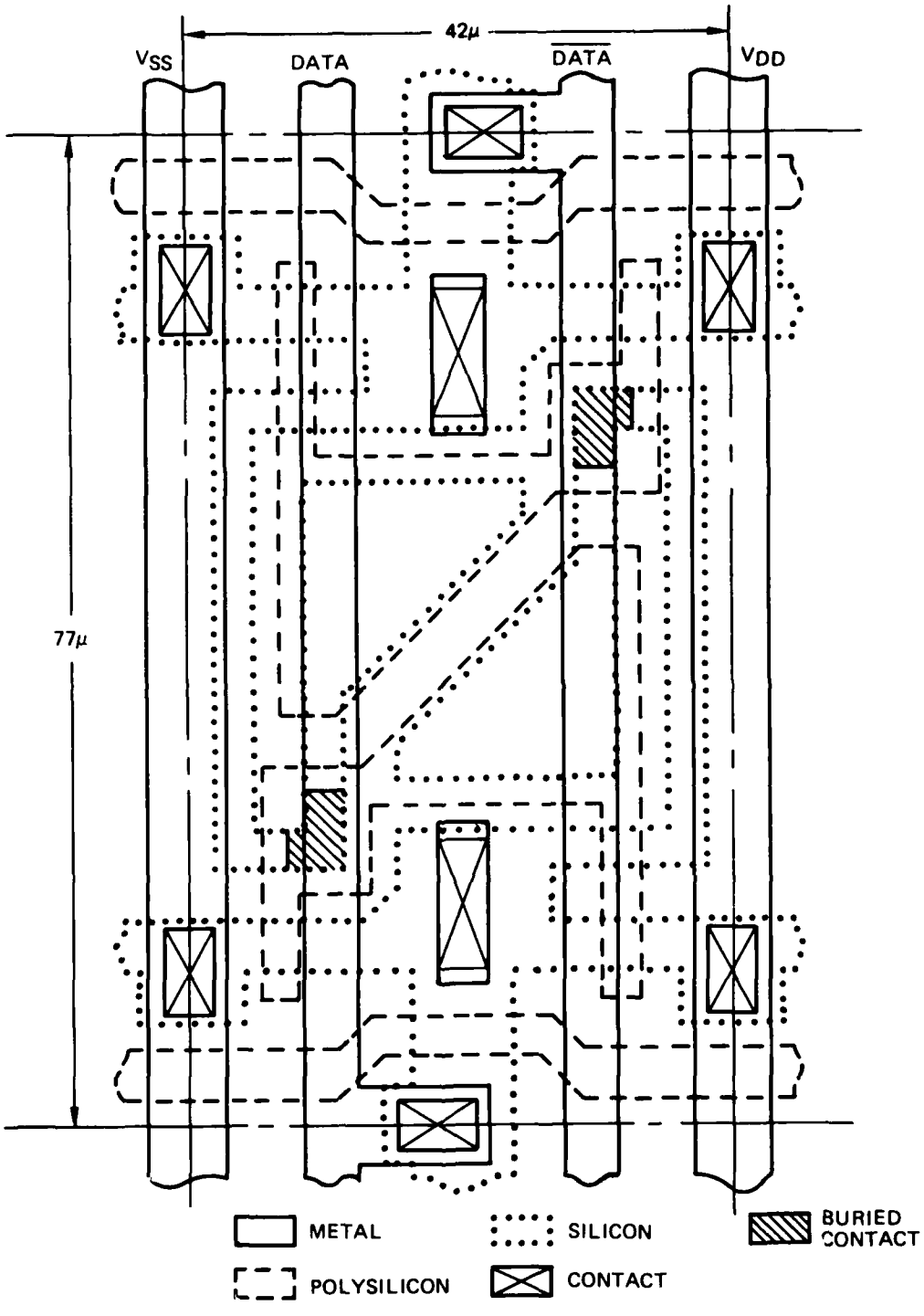

Figure 5. Memory Cell

Table 2. Process Parameters

	INITIAL	TEMP	TOTAL DOSE	
V_{TP}	1 ± .2	±.3	+ 0 - 1	VOLTS
V_{TN}	1.5 ± .2	±.3	+.5 -1.0	VOLTS
μ_P	170	120	100	cm^2/V-sec
μ_N	360	250	200	cm^2/V-sec
I_{DSP}	<10	<10	< 1	nA/μm
I_{DSN}	< 1	<10	<10	nA/μm
BV_{GO}	>30 Volts			
BV_{DSS}	>13 Volts			

N_A	4×10^{15}	
N_D	1×10^{16}	
CH_L	3 μ	
T_{OX}	600 Å	
C_{OX}	5.7×10^{-8} F/cm^2	
C_{OVLP}	2×10^{-16} F/μm	
C_{COV}	0.6×10^{-16} F/μm^2	
C_{CAP}	1.3×10^{-7} F/cm^2	(300/100)
T_{Si}	0.5 μm	
C_J	0.2×10^{-16} F/μm^2	

SHEET RESISTANCE

P^+	< 200 Ω/□
N^+	< 100
POLY	< 100
RESISTOR (P^+)	2 kΩ/□

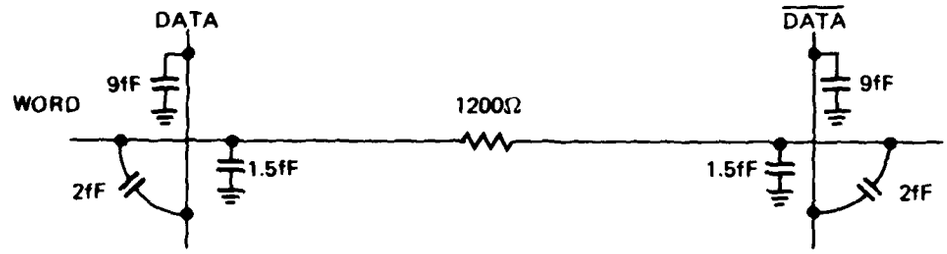

Figure 6. Memory Cell Parasitic Resistors and Capacitors

V. DECODE CIRCUITRY DESIGN

The decode circuitry is simply a one-of-N selector. Selection can be implemented in several different ways. Because it is desired to achieve high radiation levels, a full CMOS type NAND structure was chosen to implement the one-of-N selector in this design. Since the size of a CMOS NAND gate increases dramatically as the fan-in increases, it was decided to limit the fan-in to four as shown in Figure 7. The full CMOS NAND circuit maximizes the hardness to transient radiation pulses while minimizing the effects of any radiation-induced leakages.

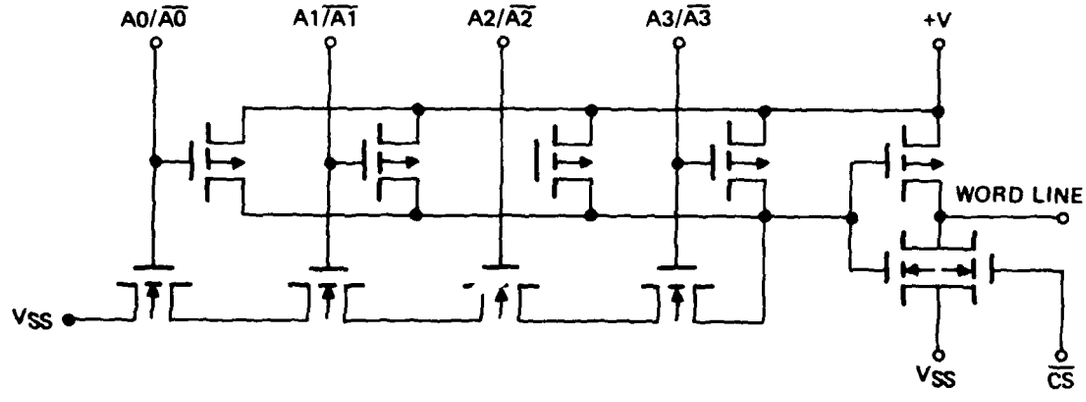

Figure 7. 1 of 16 Address Decoder

The restricted fan-in limits the decoders to one-of-sixteen and suggests an internal chip organization as shown in Figure 8. This organization also minimizes the number of transfer devices on any data line and hence, also minimizes the accumulative effect of radiation-induced leakages in these transfer devices.

VI. SENSE CIRCUITRY DESIGN

The sense circuitry in memory systems has, historically, been most sensitive to radiation effects. Radiation-induced leakage currents decrease the logical one and increase the logical zero level in the cell. For a single supply-voltage source, the signal amplitudes on the gates of the transmission devices are modified by approximately the same amount as the cells logic levels, due to leakage currents and charge coupling. Consequently, on the inputs of the sense amplifier, either the zero level is increased by the amount of the p-channel threshold voltage (if the cell is designed with p-channel transmission gates) or the one level is decreased by the amount of the n-channel threshold voltage (when n-channel transmission devices are used). Imbalances (as a superimposed result of sense amplifier offsets, nonsymmetrical leakages on the data and sense lines, and other electrical and spatial effects) can be opposite to those of the stored logic levels, with respect to the effective input voltage of the sense amplifier. Charge transfer from the data and sense lines (associated with transient currents from the pre-charge voltage source and with capacitive coupling from the selector and pre-charge rails) results in transient (10 nsec - 80 nsec) logic margin reduction, and must also be considered for high-speed operation. Finally, pre-charge voltage variations up to $\pm 10\%$ (due to process, temperature, supply and radiation effects) narrow the available zero and one margins.

Because of the indicated sensitivity to various effects, a considerable amount of development and analysis effort was devoted to the sense, read an write circuitry, to provide low offset voltage and current, high input sensitivity and large output voltage swing.

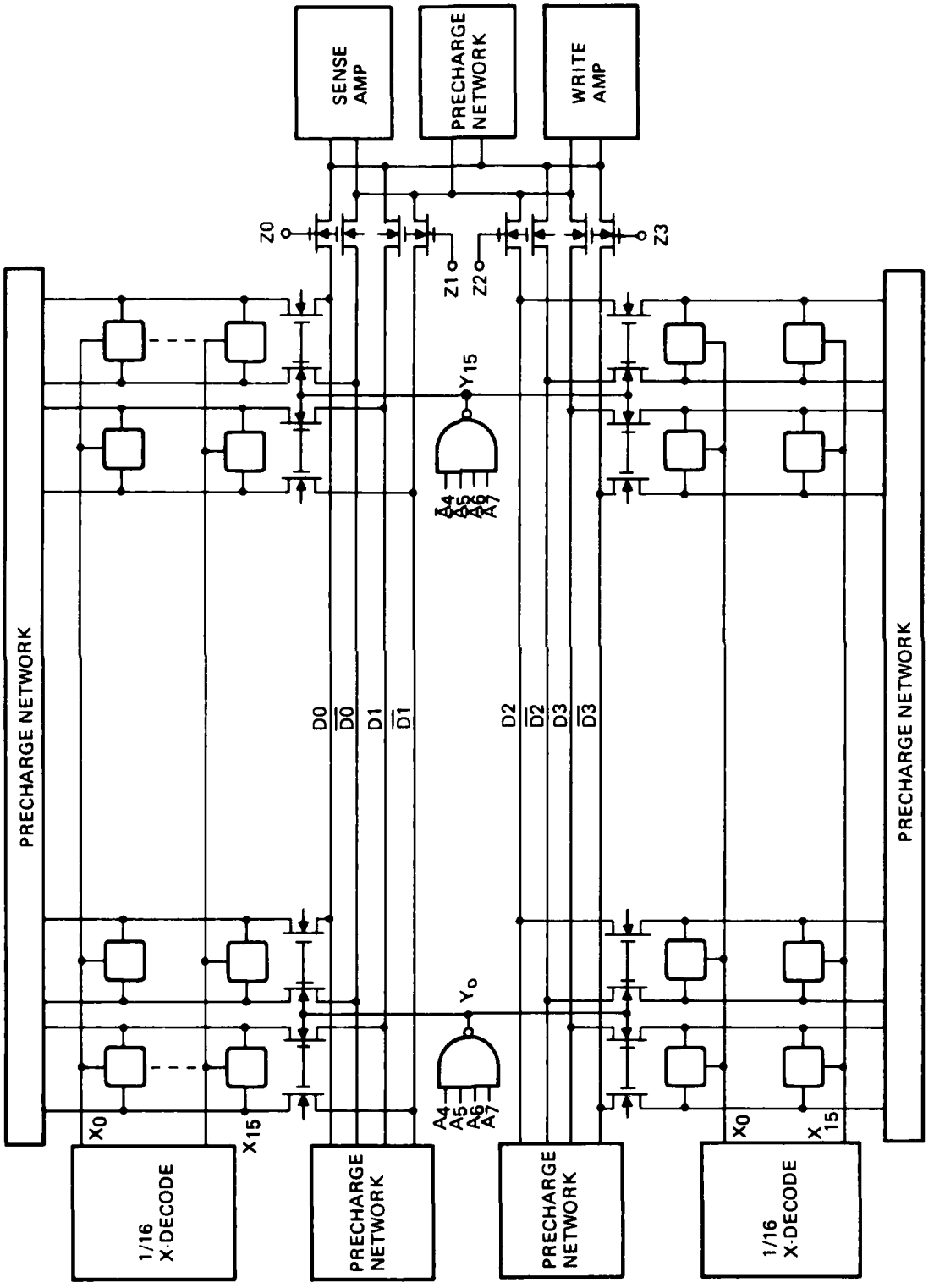

Figure 8. Bit Line Decoding Scheme

Several sense circuits that have very high-speed regenerative gain stages were considered in detail.[12] These circuits require several different clocks to operate, and some of the internally generated clocks would have critical timing requirements. Detailed analyses showed that it would be very difficult to maintain critical timing pulses through the required radiation levels and temperature and power supply voltage ranges. Additional studies were performed to consider compensation for the changes induced by temperature, radiation, and power supply voltage variations. All of the results indicated that the high-speed operation can be maintained for devices with reduced requirements for temperature ($0 \rightarrow 70°C$), radiation [<100 krads(Si)], and power supply voltage variations. For these types of sense circuits, then, some undesirable tradeoffs are required.

A second approach was investigated and subsequently chosen for the sense circuitry. This approach generally involves the use of a high-gain high-speed differential amplifier with a high common-mode operating range as the sense amplifier. In this scheme, the amplifier need only be clocked "on" with chip select (for power savings) and will respond to the voltages on the data lines as they appear. As the data stored in the memory cell overcome the precharge levels on the data lines, the amplifier responds and yields valid data. The schematic of the sense amplifier is shown in Figure 9. This amplifier is a variation of the high-speed high-gain amplifier developed for a previous program concerned with radiation-hardened CMOS/SOS comparators.[13] The circuit is extremely tolerant of temperature, voltage and radiation-induced variations. An analysis of the speed of this circuit, under worst-case conditions, shows a delay of only 30×10^{-9} seconds. This delay time is entirely satisfactory and, at worst, is a factor of three slower than the best clocked sense amplifier designs.

VII. SUMMARY

The conceptual design of a 1024-bit silicon-gate CMOS/SOS state retention random access memory has been performed. An overall topological layout for the 1024-bit memory is shown in Figure 10. Using the design rules described in Appendix I, the chip size is approximately

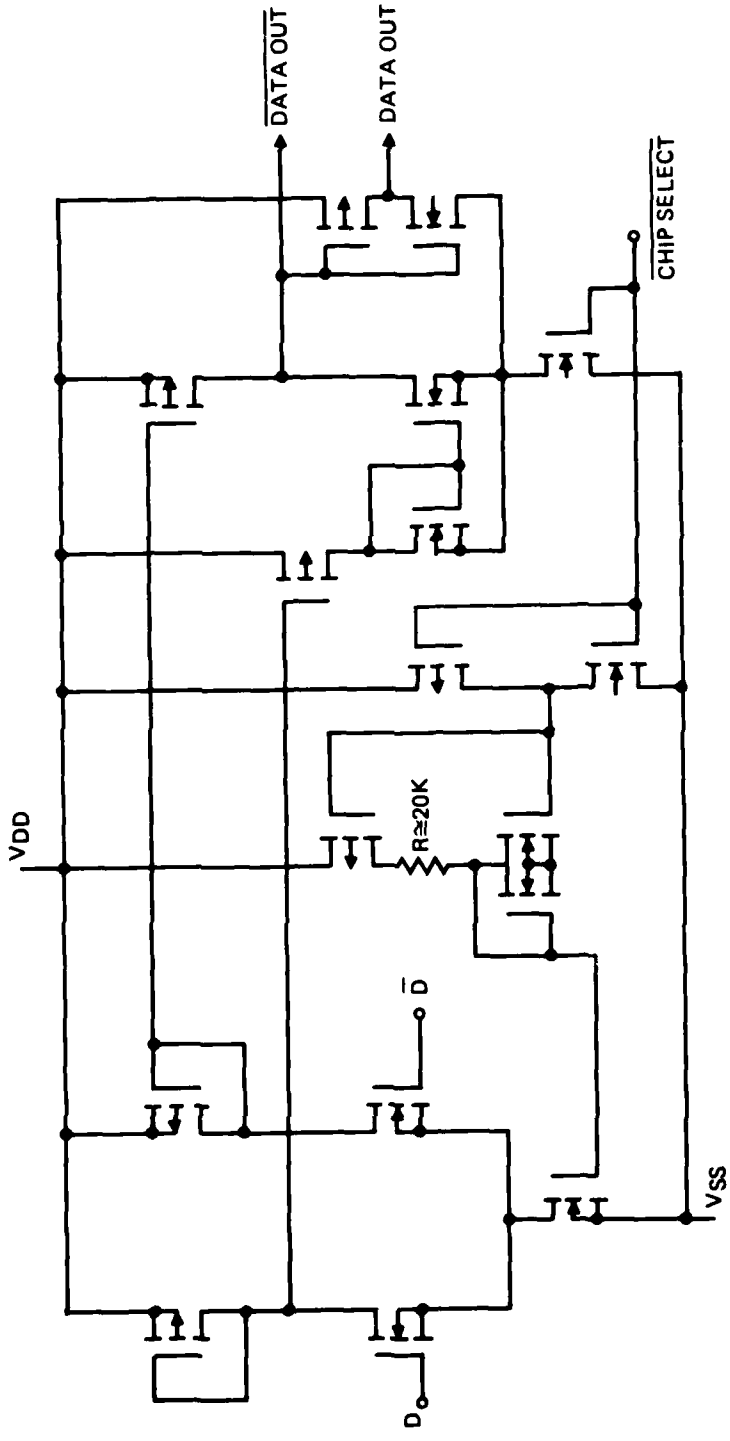

Figure 9. Sense Amplifier

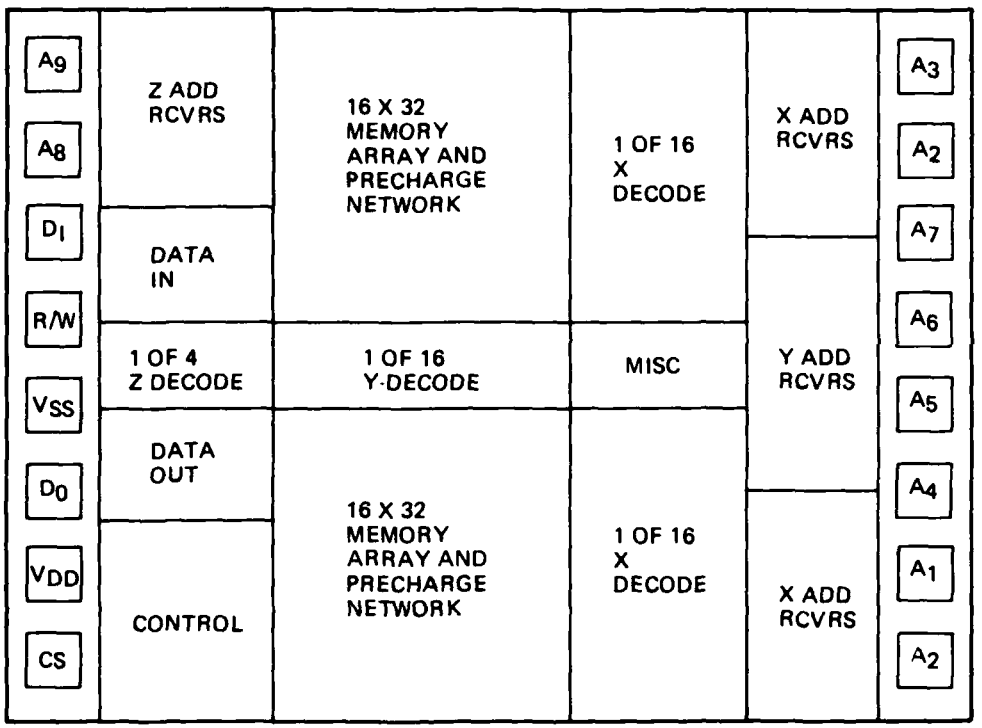

Figure 10. Topological Layout

125 mils^2. The speed and radiation goals shown on Table 1 are compatible with the design described above. Key considerations involved in the design and layout of the memory cell, decode circuitry, and sense amplifier have resulted in approaches which maximize radiation hardness while maintaining reasonable speed and density.

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APPENDIX I

CMOS/SOS MEMORY DESIGN RULES

		Min. Dimensions (μm)
1.0	**Island Mask**	
1.1a	Island Width (Base of Island)	3
1.1b	Island Width (Base of Island in Active area)	4
1.2	Island-Island Spacing	4
1.3	Buried Contact Area	6 x 6
2.0	**P-Well Mask**	
2.1	Island Overlap	2
2.2	Poly Gate Overlap (n-Channel)	2.5
2.3	Spacing from Poly Gate (p-Channel)	2.5
2.4	Spacing from Opposite Island	2
3.0	**Resistor Implant Mask**	
3.1	Island Overlap	2
3.2	Spacing from Poly Gate (n-Channel)	6.5
3.3	Spacing from Opposite Island	2
3.4	Buried Contact Overlap	3
4.0	**Buried Contact Mask**	
4.1	Contact Window to Poly Edge on Island	2.5
4.2	Contact Area	2.5 x 2.5
4.3	Contact Window Overlap at Island Edge	2.0
4.4	Spacing to Adjacent	2
4.5	Spacing to Poly Gate (on same island)	3
4.6	Contact to Contact Spacing	4
5.0	**Poly Gate Mask**	
5.1	Poly Width	3
5.2	Poly-Poly Spacing	4
5.3	Poly Extension Over Island at Gate	2
5.4	Poly-Island Spacing (long runs)	1.5
5.5	Poly-Metal Spacing (long runs (for capacitance reasons)	1.5
5.6	Poly Area for Metal Contact	7 x 7

		Min. Dimensions (μm)
6.0	**n^+ or p^+ Implant Mask**	
6.1	Island Overlap	2
6.2	Spacing from Opposite Island	2
6.3	p^+ to Poly Overlap over Buried Contact	2.5
6.4	p^+ to n^+ Overlap for Diode	3
6.5	p^+ or n^+ to Opposite Gate	4.5
7.0	**Metal Contact Mask**	
7.1	Contact Window Size	4 x 6 or 5 x 5
7.2	Contact Area	3 x 3
7.3	Spacing to Island Edge	0
7.4	Spacing to Poly Edge	1
7.5	Contact Window Size for Double Contact (n^+ to p^+ or poly to n^+ or p^+)	9 x 4
7.6	Contact Window Spacing to Gate	3.5
8.0	**Metal Mask**	
8.1	Metal Width	4
8.2	Metal-Metal Spacing	6
8.3	Metal Overlap of Contact Window	1, except 0 for internal shorting contacts
8.4	Bonding Pad Size	135 x 135
8.5	Bonding Pad to Bonding Pad Spacing	65
8.6	Bonding Pad to Unrelated Metal Spacing	40
9.0	**Glassivation Mask**	
9.1	Bonding-Pad Window Size	125 x 125

APPENDIX II

RADIATION HARDENED CMOS/SOS MEMORY PROCESS

The following description outlines a candidate radiation-hardened CMOS/SOS memory process. Only major processing steps are included, and the results of those steps are presented. In some cases, the results of several steps are combined for brevity. Some general process features that should be noted are the minimization of high temperature and thermal oxidation steps, and the restriction of all process temperatures to 900°C and below.

1 - Formation of Mask for Island Etch: Combination of thermal and deposited oxides.

2 - Island Mask: Photoresist, expose, develop, etch oxides, strip resist.

3 - Etch Islands: Use anisotropic etch to define isolated silicon islands.

4 - P-Well Mask: Thick photoresist, expose, develop.

5 - Ion Implant P-Wells: Boron ion implant to determine threshold and breakdown of n-channel transistors--strip resist, etch all oxides.

6 - MNOS Capacitor Formation: Thin thermal oxide + deposited silicon nitride.

7 - Capacitor Mask: Photoresist, expose, develop, etch nitride--strip resist, define capacitor and resistor areas in nitride.

8 - Resistor Mask: Photoresist, expose, develop, open resist over resistor areas.

9 - Implant Resistors: Boron ion implant into silicon to reduce resistivity of exposed areas to approximately 2000 Ω/□, strip photoresist.

10 - Grow Gate Oxide: Hardened gate oxidation and anneal to grow approximately 700 Å of gate oxide.

11 - Buried Contact Mask: Photoresist, expose, develop and etch oxide to form buried contacts to epitaxial silicon, strip resist. Polysilicon is then deposited using a CVD process.

12 - Polysilicon Gate Mask: Photoresist, expose, develop and etch polysilicon using plasma etching techniques, strip resist.

13 - P^+ Mask: Thick photoresist, expose, develop - define areas that form the P^+ sources, drains, and conductors.

14 - P^+ Implant: Boron ion implant to form P^+ conductors with resistivity of about 200 Ω/□ - strip resist.

15 - N^+ Mask: Thick photoresist, expose, develop - define areas that form the N^+ sources, drains, and conductors.

16 - N^+ Implant: Phosphorus ion implant to form N^+ conductors with resistivity of about 100 Ω/□ - strip resist.

17 - Deposit and Densify Field Oxide: Low pressure CVD hot wall process - about 6000 Å of silox is densified at 875°C.

18 - Contact Mask: Photoresist, expose, develop and etch oxide to form contact holes to the epitaxial silicon and the polysilicon - strip resist.

19 - Deposit Metal: Deposit about one micron of aluminum or aluminum-silicon alloy.

20 - Metal Mask: Photoresist, expose, develop, etch aluminum - strip resist.

21 - Deposit Scratch Protection: Deposit approximately 5000 Å silox at temperatures below 500°C. A sintering of the metal silicon contacts is performed during and subsequent to this operation in an inert environment.

22 - Scratch Mask: Photoresist, expose, develop and etch the protective silox coating from over the bonding pads - strip resist.

APPENDIX III

SILICON GATE CMOS/SOS RADIATION RESULTS

The radiation performance of silicon gate CMOS/SOS devices made at the Electronics Research Center of Rockwell International has been consistently good over the past 1-1/2 years. Typical ionizing-radiation-induced threshold shifts are shown in Figures 1 through 4, for a 730 Å gate oxide thickness. The results for a 580 Å gate oxide thickness are shown in Figures 5 through 8. The radiation response of the 580 Å gate oxide devices averages about .62 of the radiation response of the 730 Å gate oxide. The ratio of the square of the gate oxide thicknesses is about .63.

Over the past nine months, a significant improvement has been made in the reduction of the radiation-induced n-channel back-channel leakages. The most recent results are shown in Figure 9.

Investigations to minimize the radiation-induced n-channel edge leakage are still being conducted, since we have not yet achieved the desired levels. In the interim, a special design technique can be used to eliminate edge leakage at some expense in area and speed. The best results observed to date are side channel leakages $\leq$150 nA per edge up to one megarad(Si).

The radiation-induced reduction in field-effect mobility is shown in Figures 10 and 11. Variation in gate oxide thickness has no apparent effect on the radiation-induced mobility reductions.

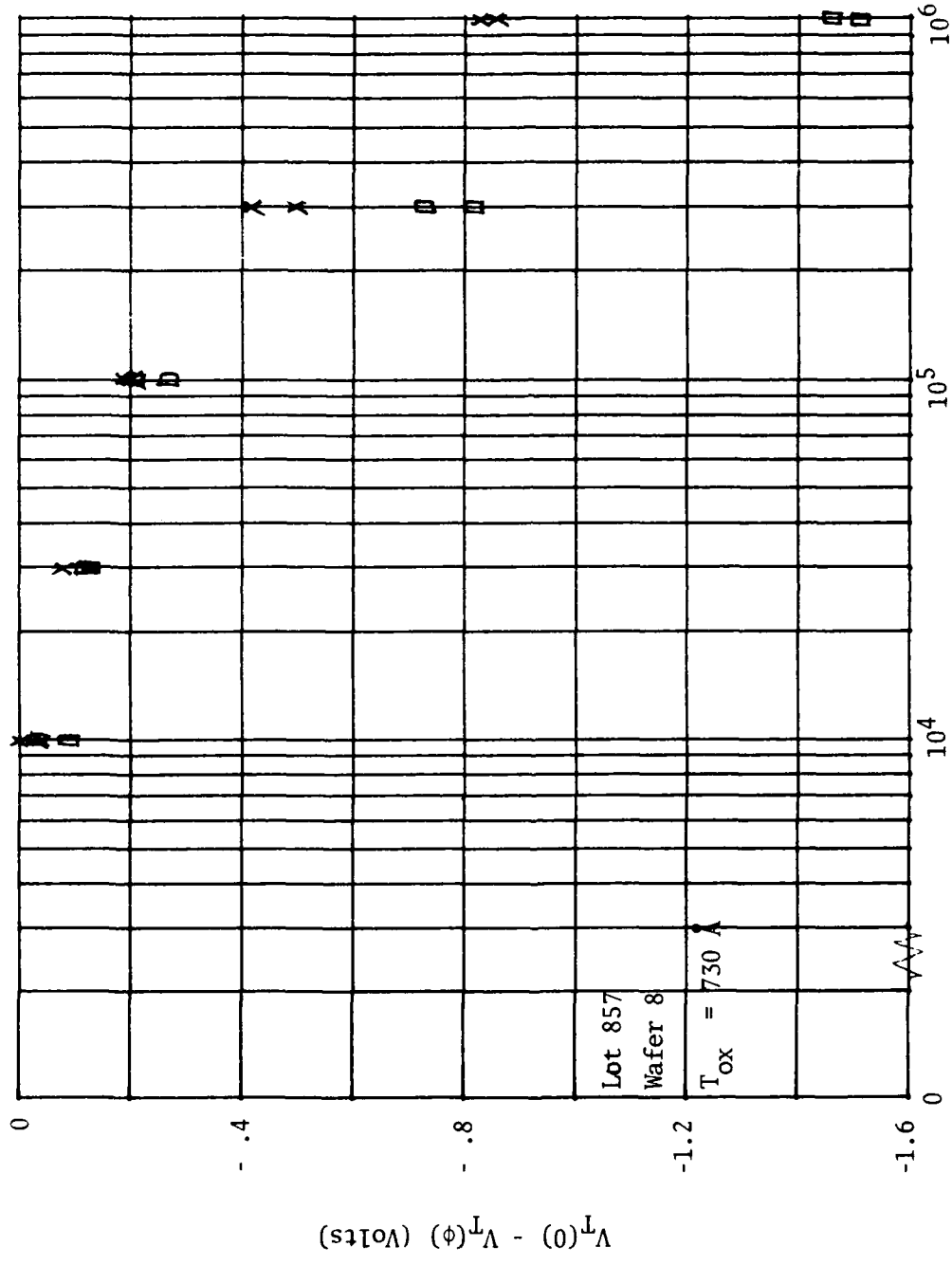

Figure 1. Radiation Induced P-Channel Threshold Shifts

X V_{GS} = -5 V_{DS} = 0

□ V_{GS} = 0 V_{DS} = -5

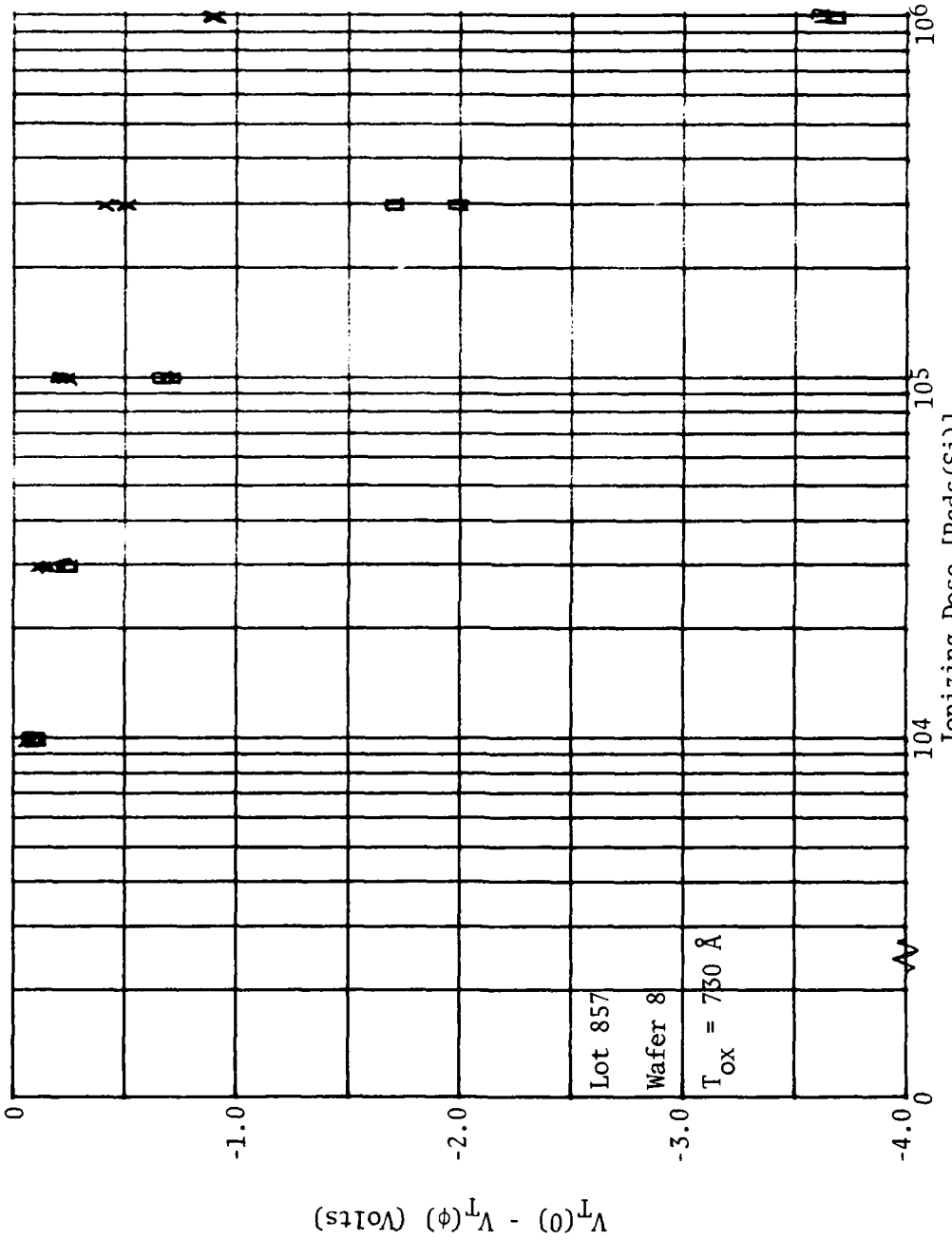

Figure 2. Radiation Induced P-Channel Threshold Shifts

X $V_{GS} = 0$ $V_{DS} = 0$

□ $V_{GS} = 5$ $V_{DS} = 0$

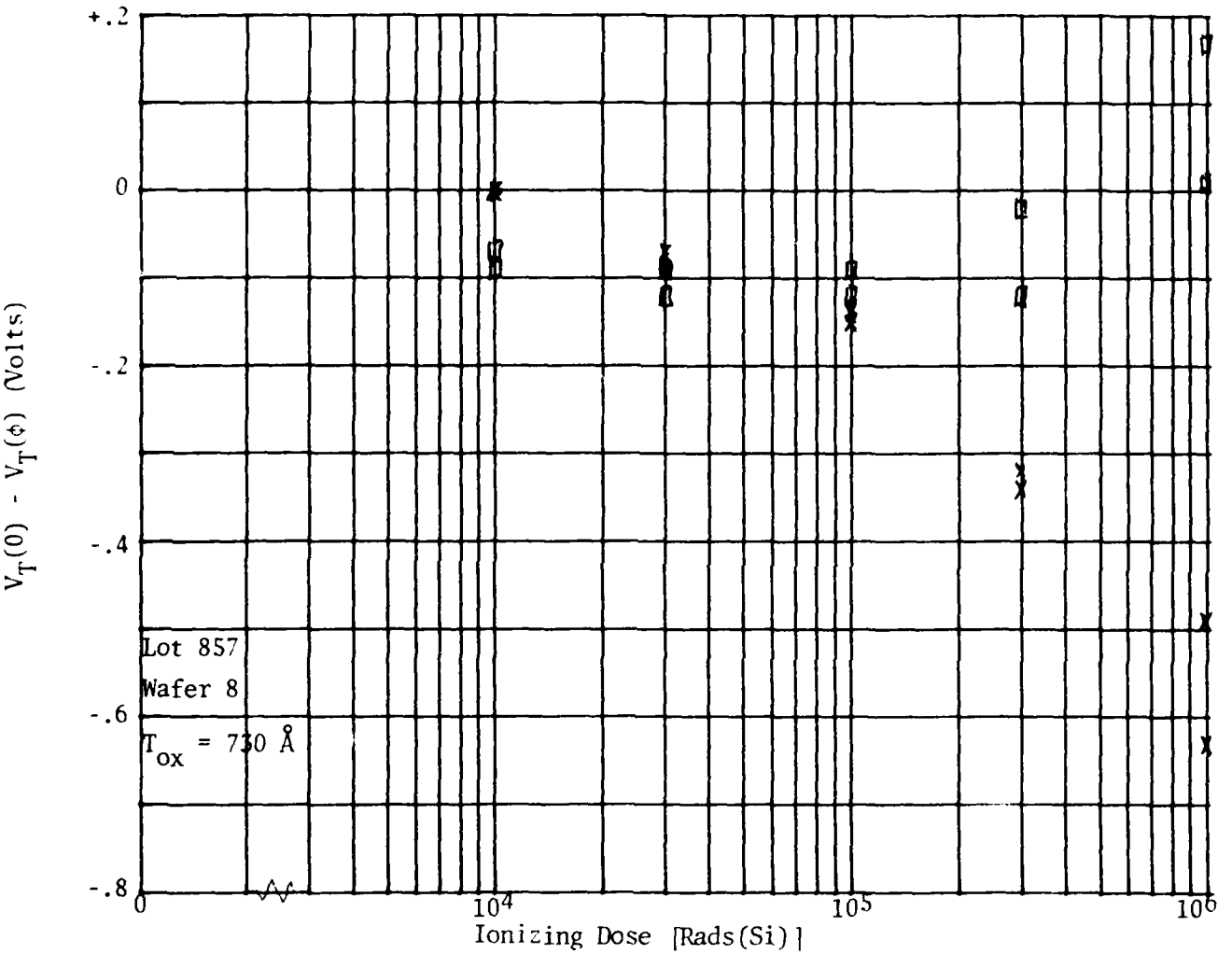

Figure 3. Radiation Induced N-Channel Threshold Shifts

X V_{GS} = -5 V_{DS} = 0

□ V_{GS} = 0 V_{DS} = 0

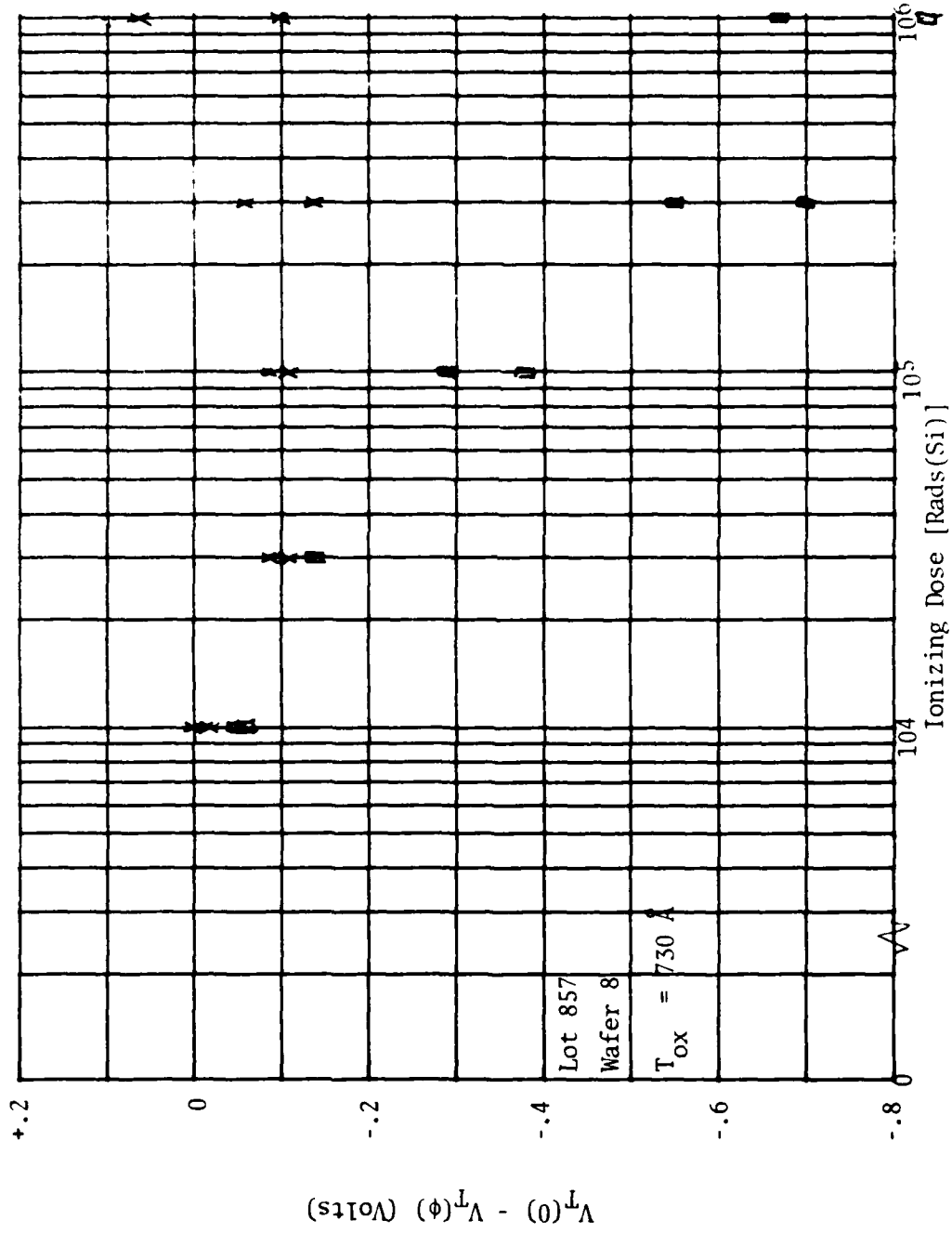

Figure 4. Radiation Induced N-Channel Threshold Shifts

X $V_{GS} = 0$ $V_{DS} = 5$

□ $V_{GS} = 5$ $V_{DS} = 0$

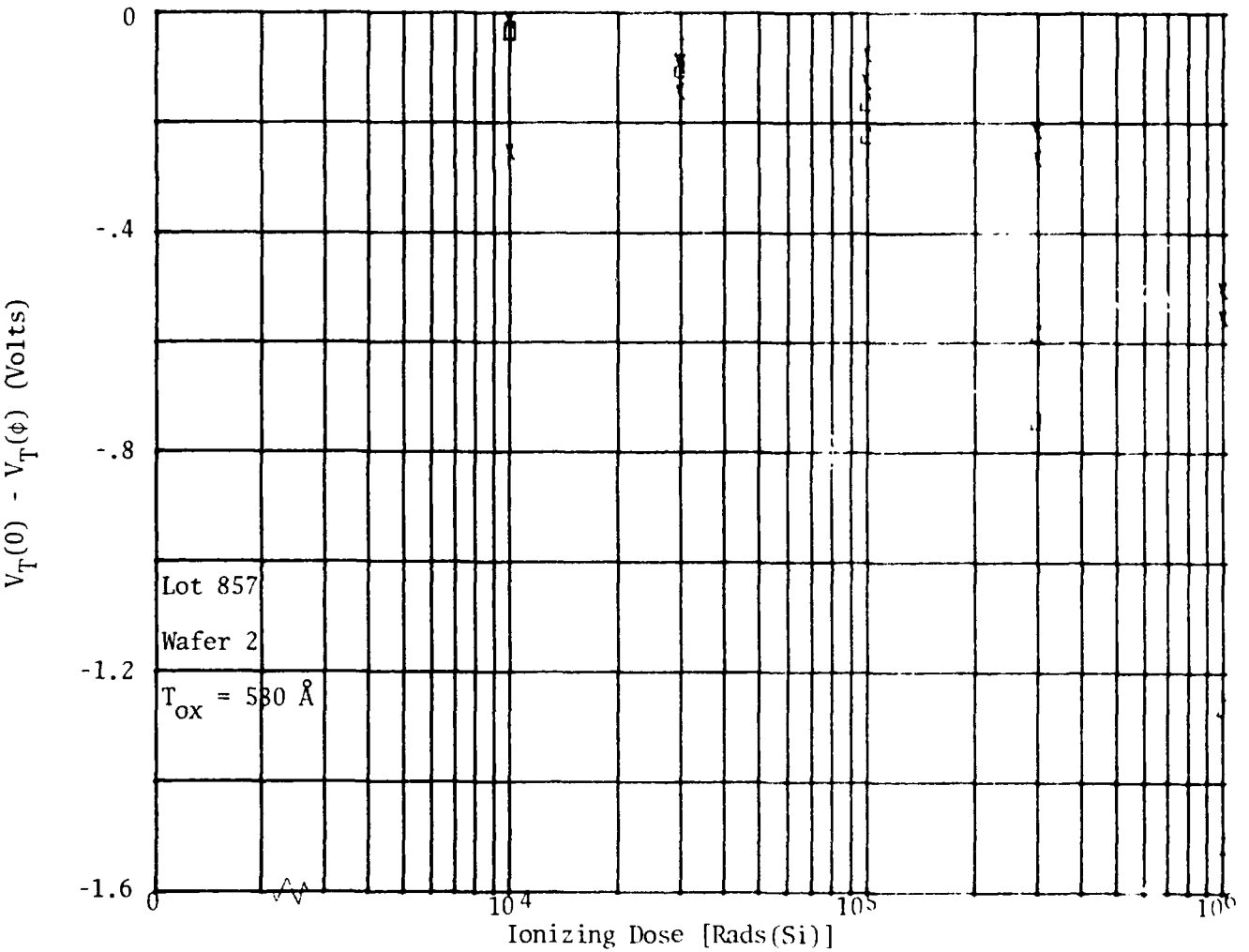

Figure 5. Radiation Induced P-Channel Threshold Shifts

X V_{GS} = -5 V_{DS} = 0

□ V_{GS} = 0 V_{DS} = -5

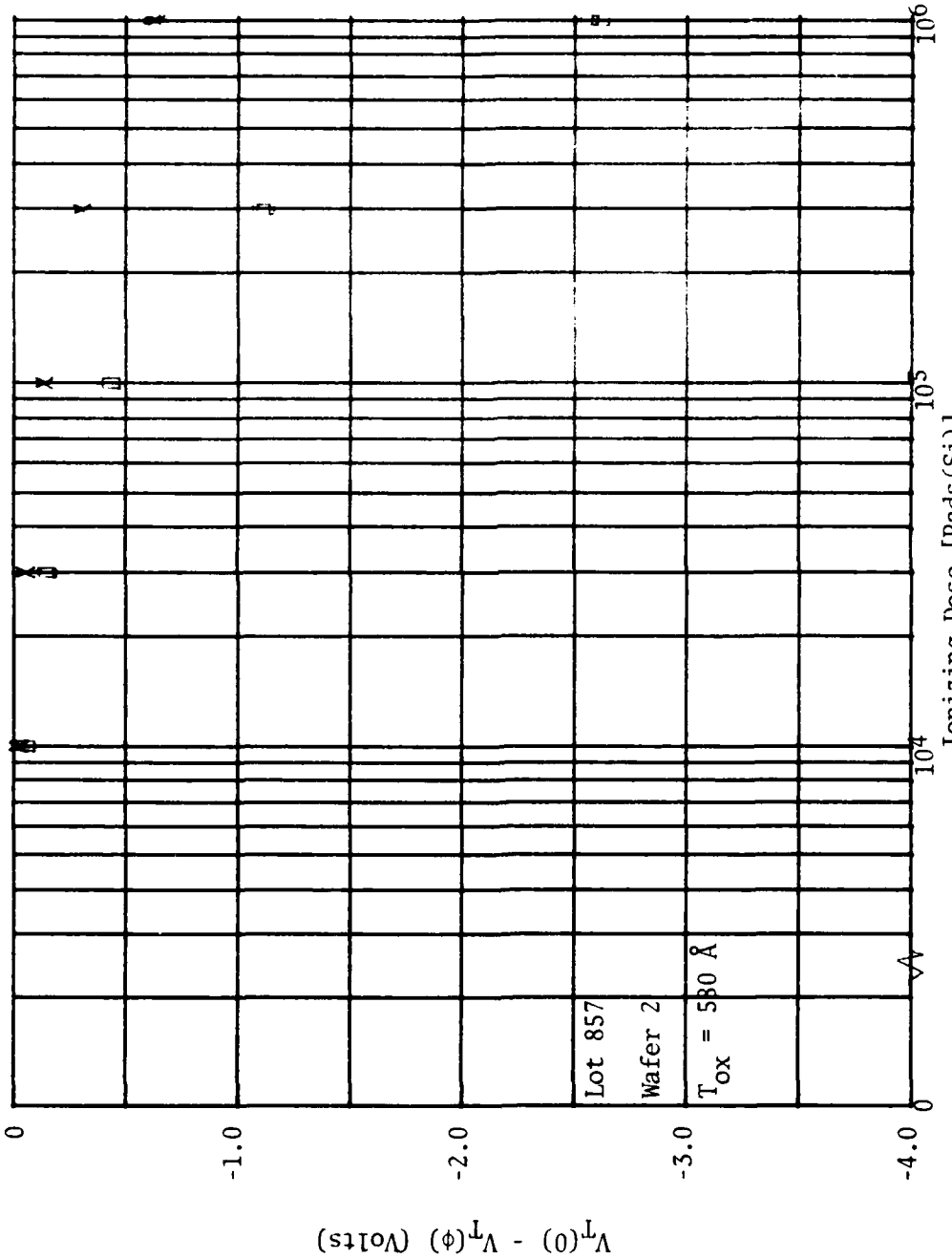

Figure 6. Radiation Induced P-Channel Threshold Shifts

X V_{GS} = 0 V_{DS} = 0

□ V_{GS} = 5 V_{DS} = 0

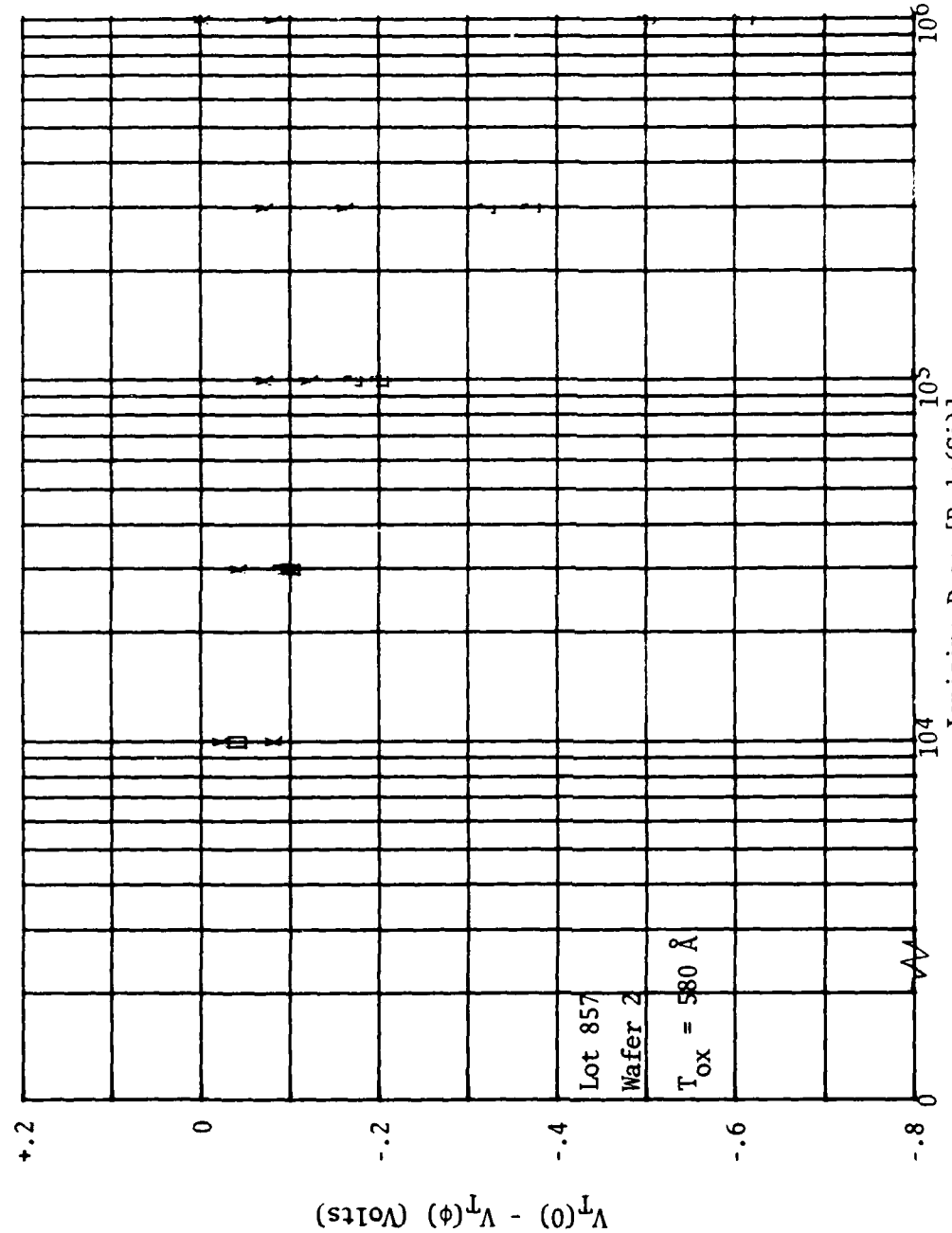

Figure 7. Radiation Induced N-Channel Threshold Shifts

X $V_{GS} = 0$ $V_{DS} = 5$

□ $V_{GS} = 5$ $V_{DS} = 0$

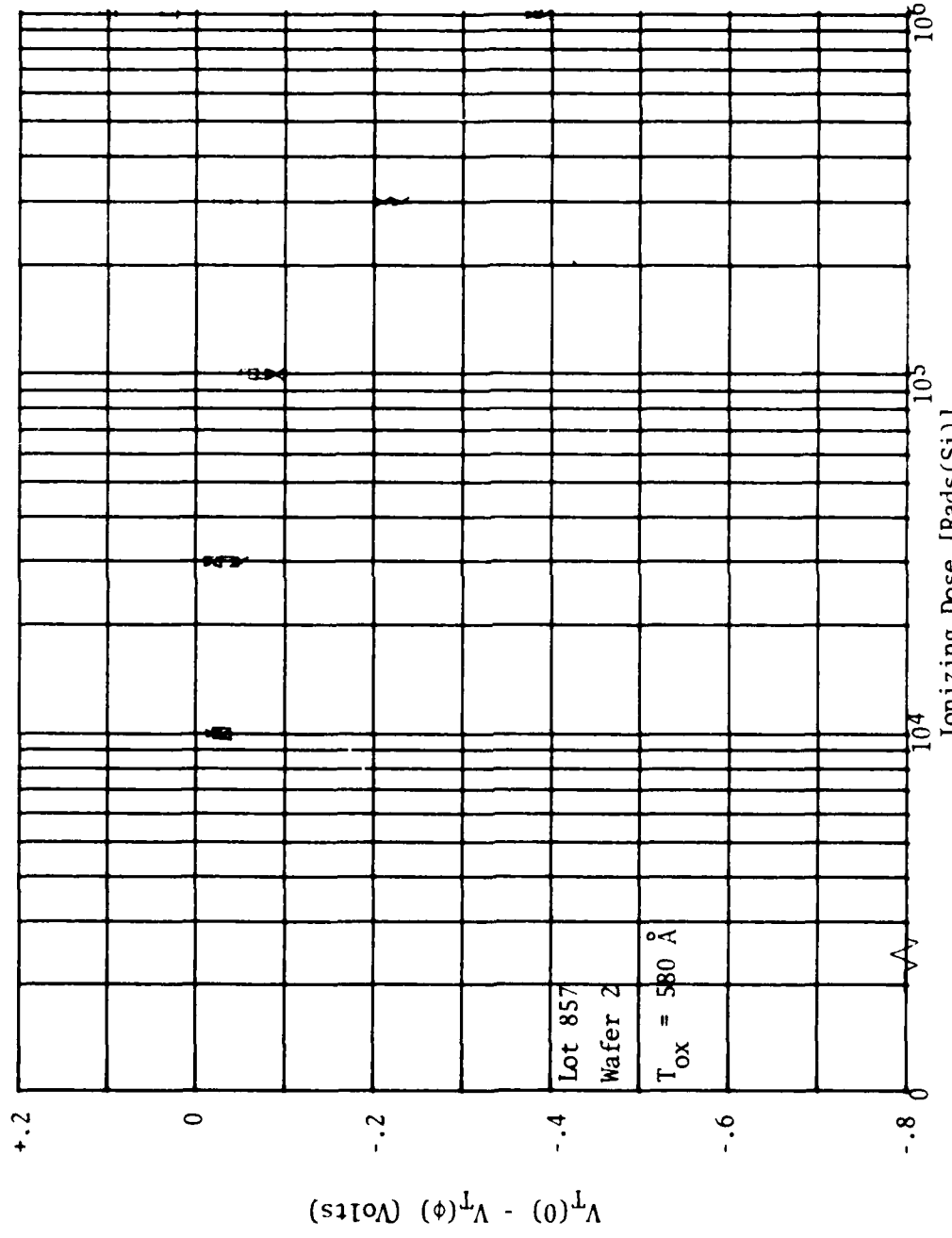

Figure 8. Radiation Induced N-Channel Threshold Shifts

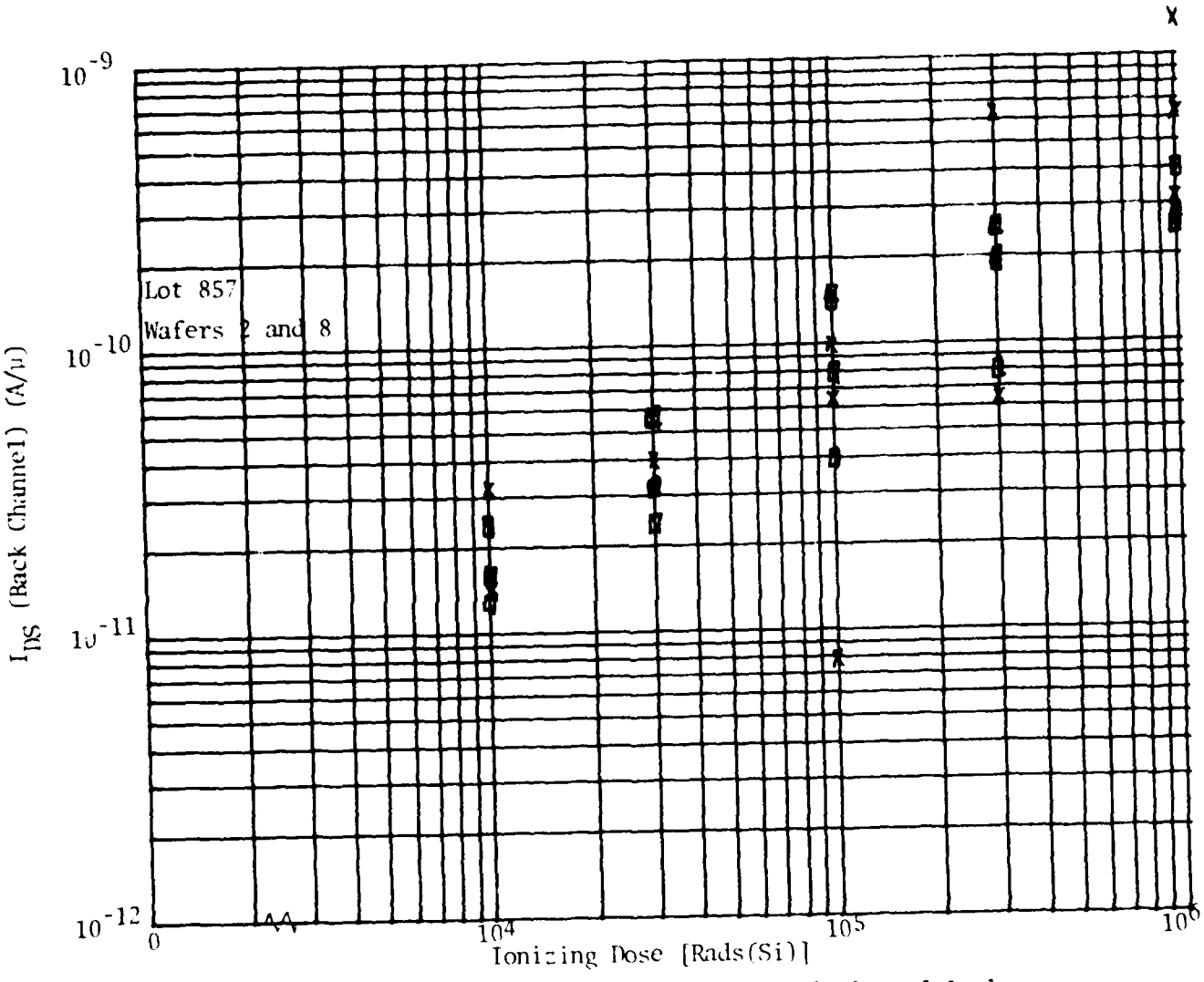

Figure 9. Radiation Induced N-Channel Back Channel Leakage

□ $V_{GS} = 0$ $V_{DS} = +5$

X $V_{GS} = +5, V_{DS} = 0$

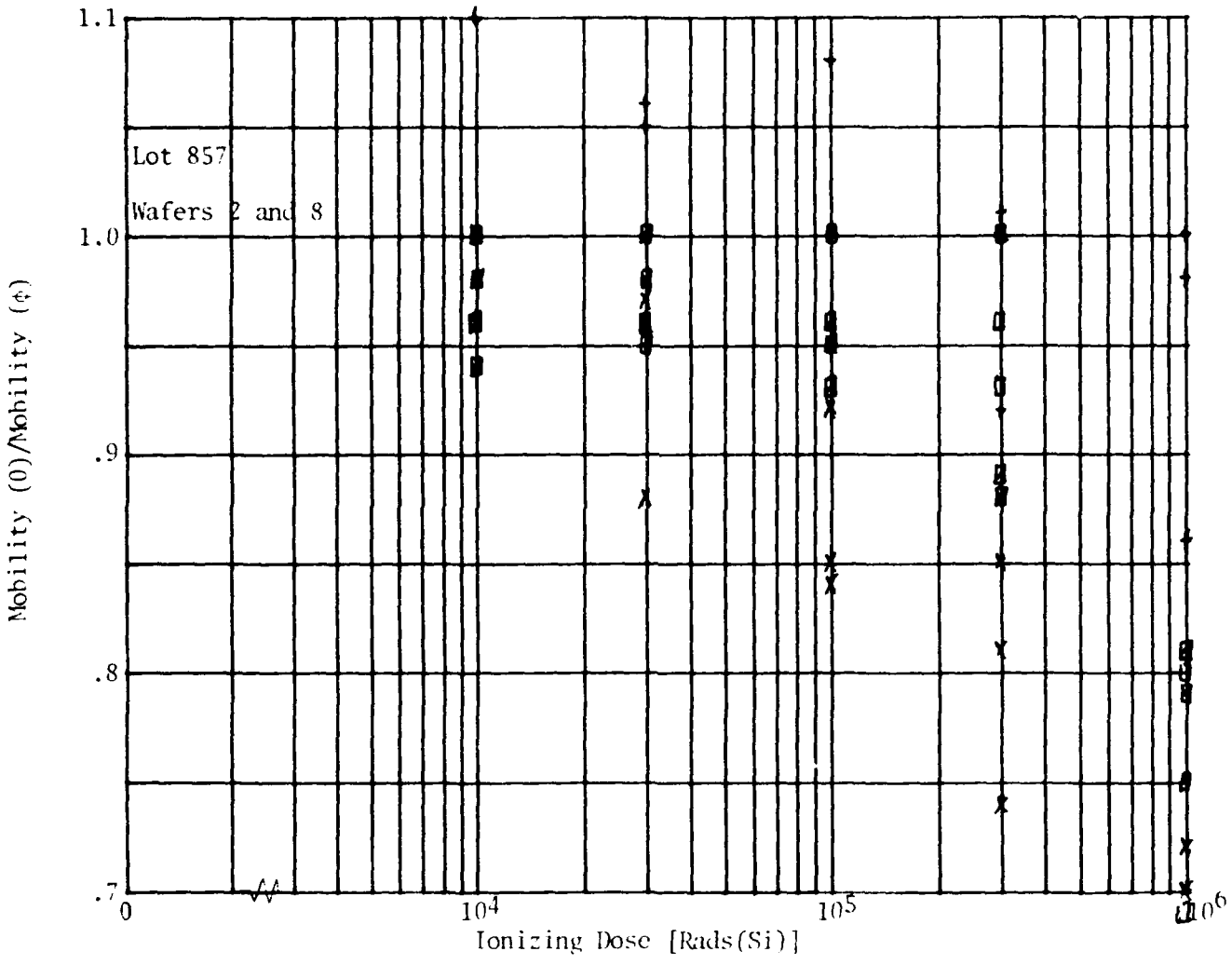

Figure 11. Radiation Induced N-Channel Mobility Changes

□ V_{GS} = 0 V_{DS} = 5 + V_{GS} = -5 V_{DS} = 0

X V_{GS} = 5 V_{DS} = 0 ⊠ V_{GS} = 0 V_{DS} = 0

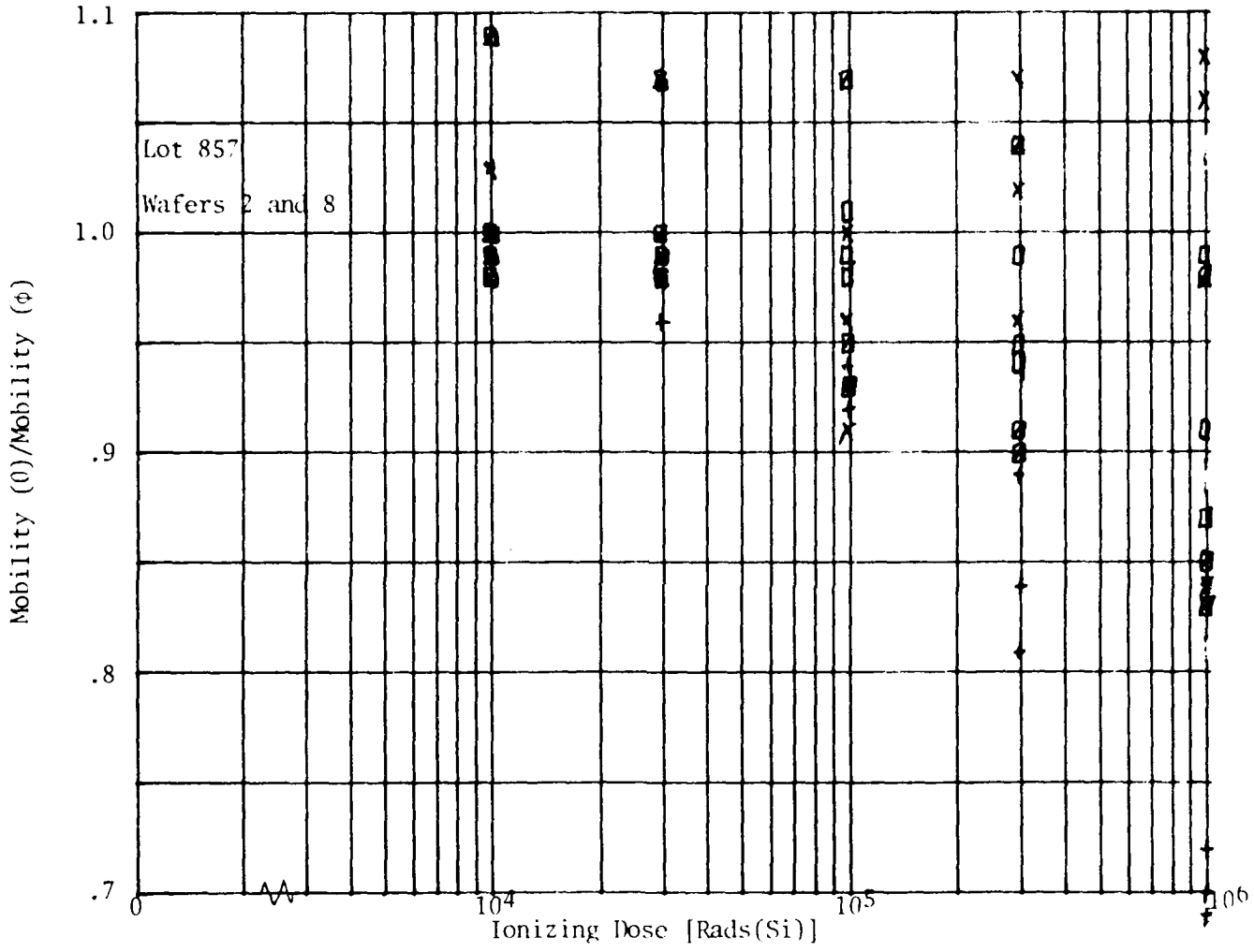

Figure 10. Radiation Induced P-Channel Mobility Changes

□ V_{GS} = -5 V_{DS} = 0 + V_{GS} = +5 V_{DS} = 0

X V_{GS} = 0 V_{DS} = -5 ⊠ V_{GS} = 0 V_{DS} = 0

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TRW Defense & Space Sys. Group
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